M90 MODULE AND 790 UNIT NUMERIC/DATA DESCRIPTOR DISPLAYS

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INTRODUCTION

The M-90 numeric/descriptor display modules provide NCR terminals with a means of displaying variable numeric information and fixed message information. The display modules can contain numerics only (M-90-1-XXX), fixed messages only (M-90-2-XXX), or combinations of both numerics and fixed messages (M-90-3-XXX). The XXX in the module number indicates the parent unit for which the module was designed.

Currently there are three models of M-90 excluding the 790 remote display: M-90-1-748, M-90-3-270, and M-90-3-280. The M-90-1-748 shown in figure 1 is a numerics-only display capable of displaying a 14 digit number. The M-90-3-270 shown in figure 2 is a combination display having 14 numeric positions and 56 fixed messages. Figure 3 depicts the M-90-3-280 which contains eight numeric positions and 24 fixed messages. The 790 remote display shown in figure 4 contains six numeric positions and 16 fixed message positions.

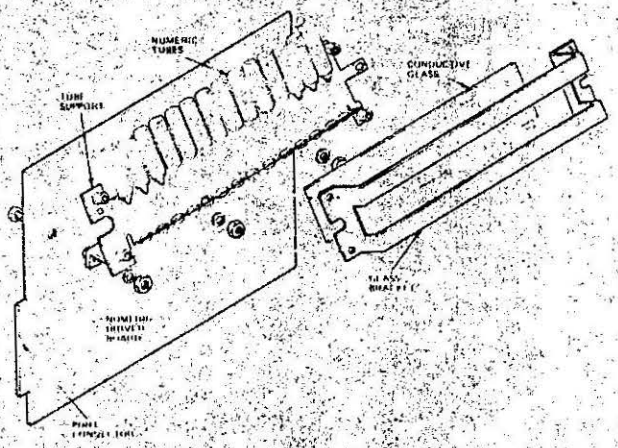

Fig. 1. M-90-1-748 display

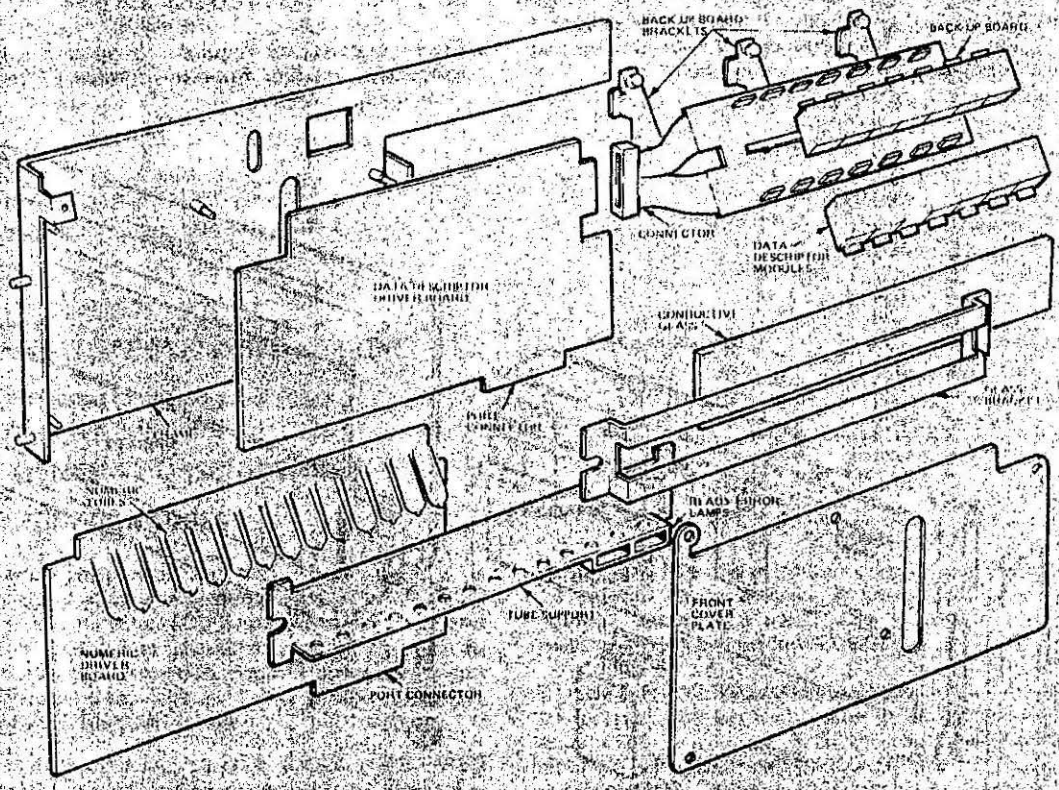

Fig. 2 M-90-3-270 display

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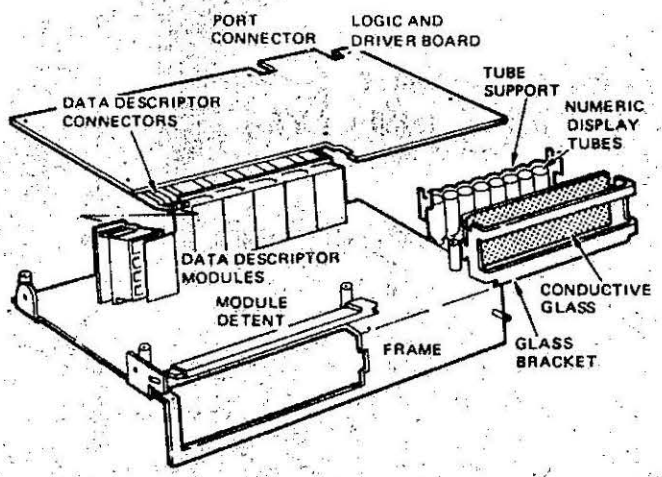


Fig. 3 M-90-3-280 display

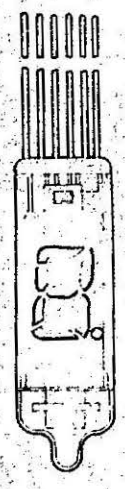


Fig. 5 Numeric tube

Numeric information is displayed using seven-segment vacuum fluorescent tubes. Refer to figure 5. A decimal point is also included to the right of the seven- segment character. The seven segments allow the display of the numbers 0 through 9 and dash (-). The maximum number of tubes per display is 14.

The fixed messages or data descriptors are displayed by lighting an incandescent lamp behind a film strip. The film strips are mounted on modules of four messages each as shown in figure 6. A maximum of 14 four-message data descriptor modules can be contained in one M-90.

The logic to control the display module operations is contained in four MOS/LSI arrays. Four arrays are required to operate 14 numeric/descriptor positions. M-90 displays containing more than 14 numeric/descriptor positions require duplicate sets of the arrays. For example, the M-90-3-270 contains 14 numeric positions and 14 four-message data descriptor modules. This module requires two sets of four MOS/LSI arrays. Each set, in turn, requires one position on the TCU common port.

Driver circuits are required to operate the incandescent lamps and vacuum fluorescent tubes of the display. The

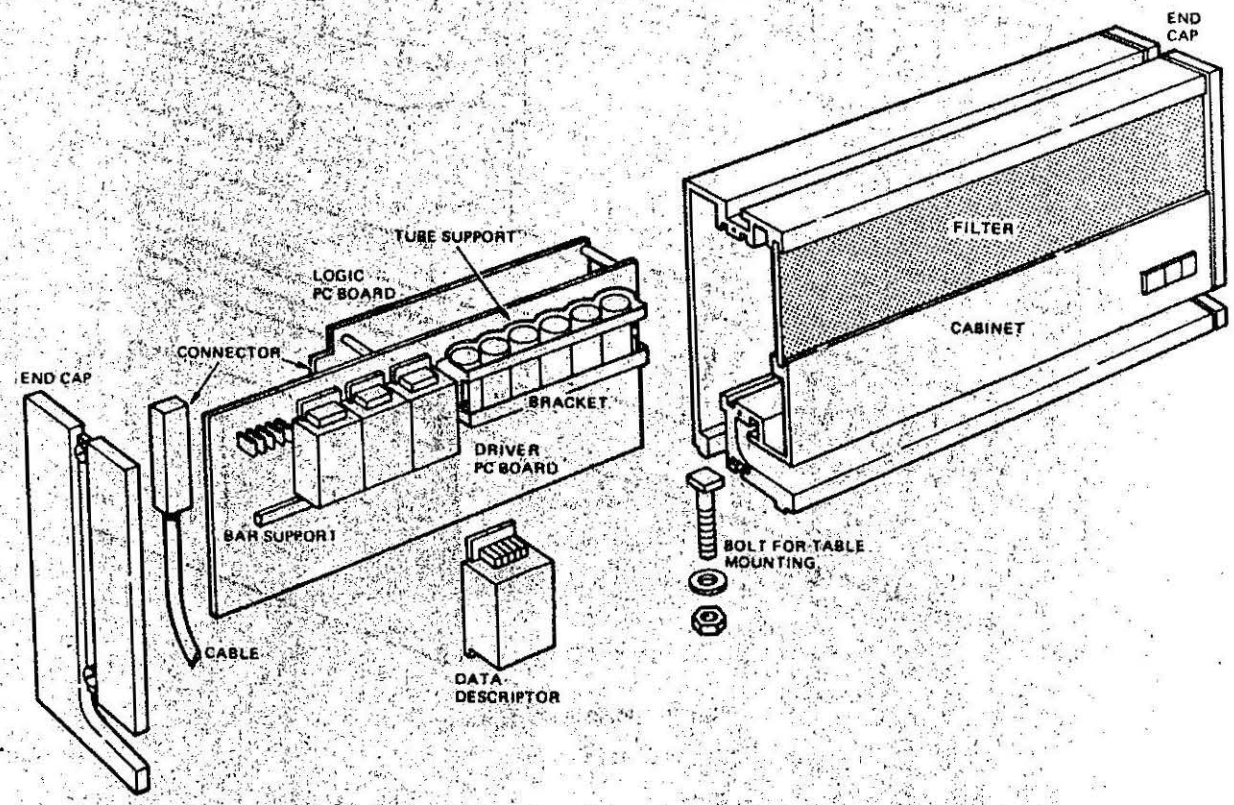


Fig. 4 790 remote display

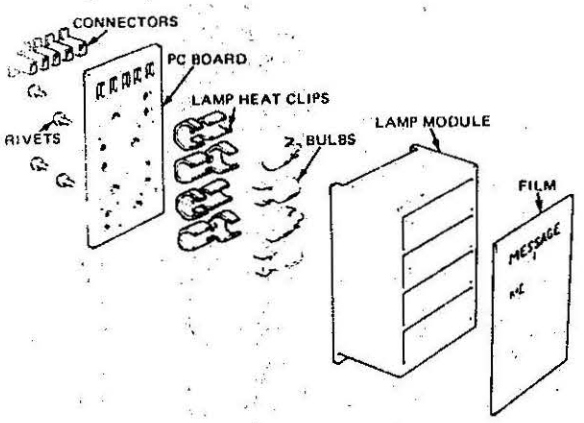


Fig. 6 Data descriptor module

driver circuits are made up of discrete components or hybrid circuit packages.

To ensure proper operation of the display modules the following power and environmental requirements must be met.

Voltage		Use
+12 v.d.c.	±5 percent	MOS and Drivers
-6.8 v.d.c.	±10 percent	MOS
-12 v.d.c.	±5 percent	MOS
+28 v.d.c.	+10 or -15 percent	Drivers
-20 v.d.c.	±10 percent	Tube anode drivers
-5 v.d.c.	±10 percent*	Tube grid drivers
3.2 v.a.c.	±10 percent*	Tube filaments

Temperature

Operating Range**	+32° to +125° F.
Storage Range	-40° to +160° F.

Relative Humidity

Operating Range	20 to 88 percent
Storage Range	20 to 88 percent

* Voltages referenced to -20 v.d.c.
** Temperature within parent unit

GENERAL DESCRIPTION

TCU-ISSUED FUNCTION CODES

The information displayed by the M-90 module is controlled by the parent unit terminal control unit (TCU). This control is provided by TCU-issued function codes and data characters. Each data character sent to the display must be preceded by a function code. The functions and the bit configurations for each are listed in table 1. A brief explanation of each function follows.

Bits 1 through 4 of the function code are ignored by M-90 function decode logic and may be either a logic ONE or a logic ZERO.

PUNCTUATE – The punctuate function causes the decimal point between the second and the third numeric characters to light. In some international machines the decimal is placed between the third and fourth numeric characters.

Function	Code b_8	b_7	b_6	b_5
Punctuate	0	0	0	1
Accept Data Descriptor Character	0	0	1	0
Accept Numeric Character	0	1	0	0
Punctuate and Accept Numeric Character	0	1	0	1
Clear Entire Display	1	0	0	0
Clear Numeric Portion Only	1	1	0	0

Table 1 M-90 function codes

ACCEPT DATA DESCRIPTOR CHARACTER – When an accept data descriptor character function is received, the M-90 prepares to accept the code for the data descriptor to be lit. The data character received following receipt of this function determines which data descriptor message is to be displayed.

M-90 displays can contain up to 14 four-message display modules. The least significant four bits of the data character following the accept data descriptor character function contains the module number or column. The one message out of four in a given column is selected by the contents of the most significant four bits of the data character. Table 2 shows the bit configurations for the data descriptor code.

b8	b7	b6	b5	b4	b3	b2	b1	
			0	0	0	1		Select Column 1
			0	0	1	0		Select Column 2
			0	0	1	1		Select Column 3
			0	1	0	0		Select Column 4
			0	1	0	1		Select Column 5
			0	1	1	0		Select Column 6
			0	1	1	1		Select Column 7
			1	0	0	0		Select Column 8
			1	0	0	1		Select Column 9
			1	0	1	0		Select Column 10
			1	0	1	1		Select Column 11
			1	1	0	0		Select Column 12
			1	1	0	1		Select Column 13
			1	1	1	0		Select Column 14
X	0	1	1					Select Row 1
X	1	0	0					Select Row 2
X	0	1	0					Select Row 3
X	1	1	0					Select Row 4
X	1	1	1					Clear Column

NOTE: X may be either 1 or 0

Table 2 Data descriptor codes

Any of the five row codes can be combined with any of the 14 column codes to select a given message or to clear a column. Selecting a message in a column turns off any message previously on in that column.

ACCEPT NUMERIC CHARACTER – The M-90 prepares to receive a numeric character code from the TCU after receipt of an accept numeric character function. The eight-bit data character following the function character determines the numeric character to be displayed. Table 3 contains the codes for the numeric display characters.

The numeric character received after the accept numeric character function is displayed in the least significant position of the numeric display. Receipt of subsequent numeric characters causes the previously displayed

CODE				CHARACTER
b4	b3	b2	b1	
0	0	0	0	(zero)
0	0	0	1	(one)
0	0	1	0	(two)
0	0	1	1	(three)
0	1	0	0	(four)
0	1	0	1	(five)
0	1	1	0	(six)
0	1	1	1	(seven)
1	0	0	0	(eight)
1	0	0	1	(nine)
1	1	0	1	(hyphen)
1	1	1	1	(blank)

Table 3 Numeric codes

characters to be shifted one position to the left until all numeric tubes are lit.

In displays containing a combination of descriptors and numeric with only 14 display positions (M-90-3-280), the numerics are shifted to the left until all numeric positions are used. Shifting numeric data into the descriptor section of the display could light more than one message in a column causing damage to the descriptor module.

PUNCTUATE and ACCEPT NUMERIC CHARACTER – The punctuate and accept numeric character function causes the M-90 to light the decimal point between the second and third numeric positions and to prepare the display to receive a numeric data character. This function is a combination of the punctuate function and the accept numeric character function.

CLEAR ENTIRE DISPLAY – After receiving the clear entire display function, the M-90 extinguishes all descriptor messages and/or numerics.

CLEAR NUMERIC PORTION ONLY – The numeric portion of the display is cleared when this function is sent by the TCU. All descriptor messages lit prior to receiving the clear numeric portion only function remain lit after the function is performed.

GENERAL OPERATION

M-90 display modules contain five general sections within the logic: data input and gating, circulating data storage, data decode and display, unit control logic, and status code generator. These five sections interact to perform the functions of the display. Refer to figure 7.

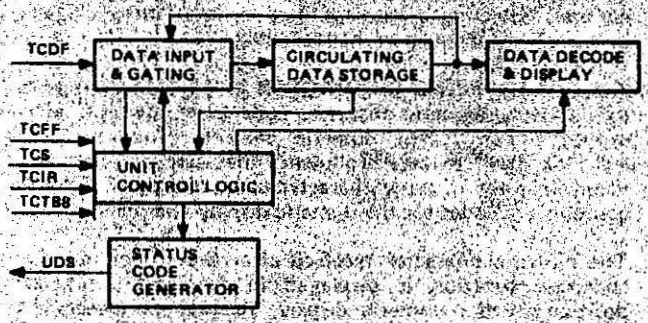


Fig. 7 Logic block diagram

The function codes are sent to the display on the TCDF line and received by the data input and gating section of the logic. The functions are decoded and stored by the unit control logic. The status is switched to BUSY upon receipt of any function except punctuate. Refer to the logic operation flow chart (fig. 8).

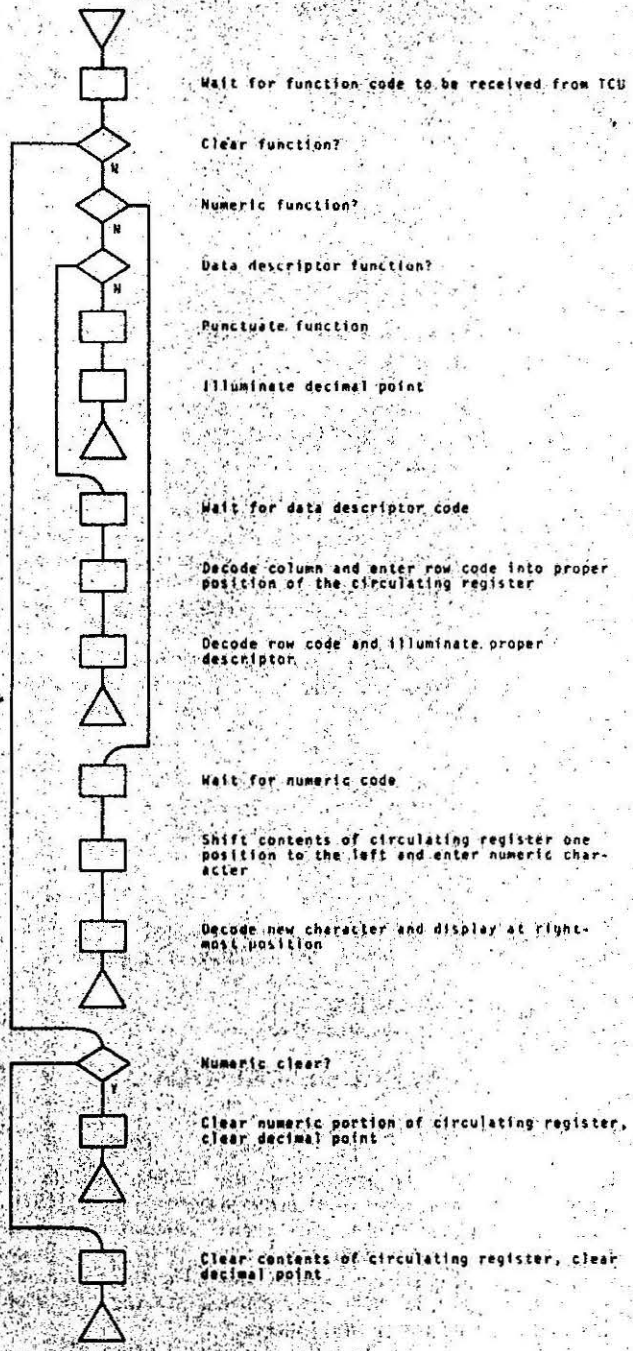


Fig. 8 Logic operation flow chart

The display waits for additional data to be sent before the function can be completed (clear functions and punctuate function excepted). When the data to be displayed is received, it is converted to a four-bit code and stored in the circulating data storage. The column in which the four-bit

character is displayed is determined by the position the character occupies in the circulating data storage. When display data is received, it is held in the data input portion until the unit control logic determines that the circulating data storage is in position to accept the character. After the character is stored, it is circulated with the previously stored data and applied to the data decode and display section. The status reverts to READY after data is entered into the circulating register.

As data characters are circulated, they are decoded and displayed. This operation is performed by the data decode and display section which is under the control of the unit control logic. The data decode handles descriptor data and numeric data in the same manner. The drive circuitry differs between the numerics and the data descriptors. This is necessary because the data descriptors are illuminated by incandescent lamps while the numerics are provided by vacuum fluorescent tubes.

LOGIC DESCRIPTION

The four MOS/LSI logic arrays of the display module perform the various operations necessary to display data received from the TCU in the proper position and at the proper time to be intelligble to the terminal operator. These operations include function decode, data entry, entry cycle, and data

FUNCTION ENTRY AND DECODE

The M-90 is controlled by function codes sent from the TCU. Some codes signal the display that display data is to be received. Other codes initiate punctuate and clear functions.

The codes are received on the TCDF line and held temporarily in the input buffer. The function code is decoded and stored in four flip-flops. Refer to figure 9. A brief description of each flip-flop follows.

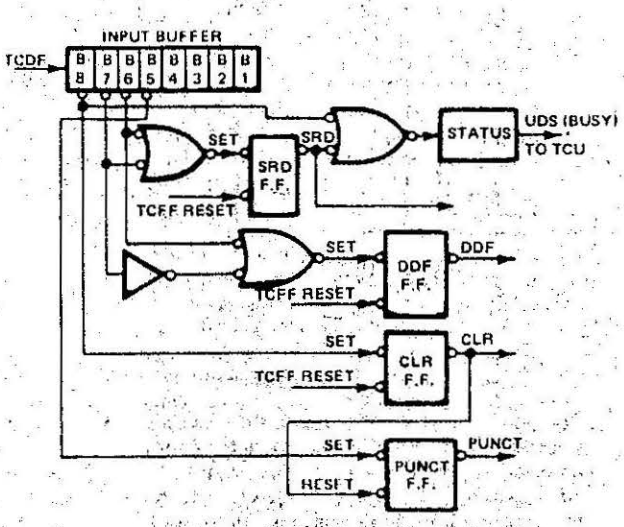


Fig. 9 Function entry and decode logic

The flow chart in figure 10 outlines the flip-flops set when each function code is decoded.

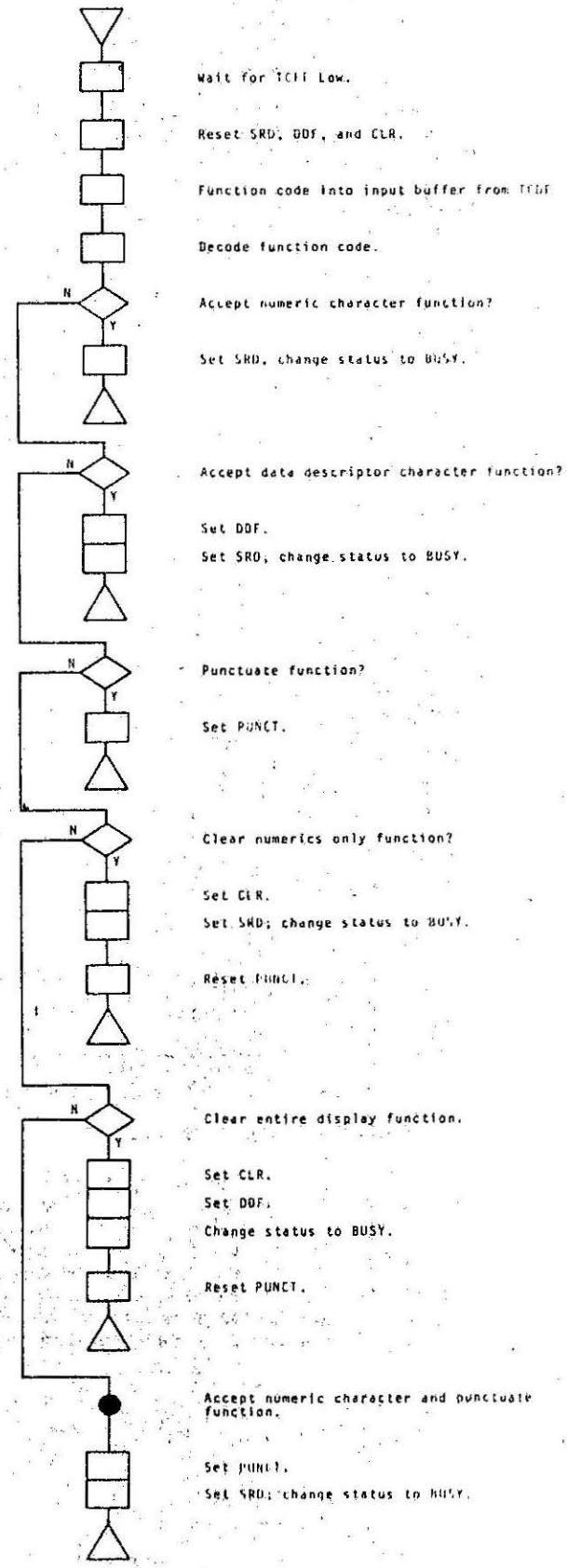


Fig. 10 Function entry and decode flow chart

CLR FLIP-FLOP – This flip-flop is set with any clear function received (clear entire display function or clear numeric portion only function).

PUNCT FLIP-FLOP – The PUNCT flip-flop is set with the receipt of either a punctuate function or a punctuate and accept numeric character function.

DDF FLIP-FLOP – The DDF flip-flop is set to indicate that the function received affects the contents of the descriptors; that is, either an accept data descriptor character function or a clear entire display function is issued.

SRD FLIP-FLOP – The SRD flip-flop is set when any of the data display functions (accept data descriptor character, accept numeric character, punctuate and accept numeric character, or clear numeric portion only) is received from the TCU. SRD switches the M-90 status to BUSY.

The SRD, DDF, and CLR flip-flops are reset when a new function is issued (TCFF active). The PUNCT flip-flop remains set after a punctuate function is received. The PUNCT flip-flop is reset by receipt of either of the clear functions or by the initial reset signal (TCIR) from the clock module.

DATA ENTRY

When an accept data descriptor character function, an accept numeric character function, or punctuate and accept numeric character function is received from the TCU, the input buffer is prepared to receive a data character from the TCU. The SRD flip-flop is set when either a numeric character or a data descriptor character is to be received. When a data descriptor character is expected, the DDF flip-flop is set along with SRD. The DDF flip-flop is reset when a numeric data character is expected.

When a numeric data character is received on the TCDF line, the character is gated into the eighth position (B8) of the input buffer (see fig. 11). The bits of the character are shifted serially into the buffer until all eight bits have been received.

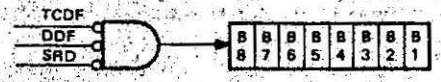


Fig. 11 Numeric data entry

A descriptor data character is gated into the fourth bit position (B4) of the input buffer (see fig. 12). The data is shifted serially into the buffer until the first seven bits have been received. The eighth bit is forced to a logic 1 by the M-90 logic. After all eight bits of the data character are transferred into the input buffer, the first four data bits received are in positions B5 through B8 of the input buffer, and the last four bits received are in input buffer positions B1 through B4.

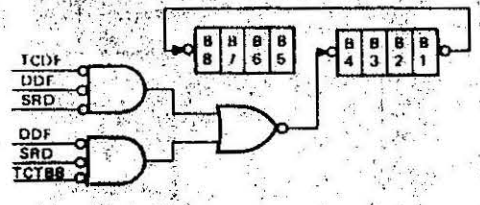


Fig. 12 Descriptor data entry

ENTRY CYCLE

After the data character is loaded into the input buffer, the contents of the input buffer must be transferred to the circulating register under the direction of the control logic (see fig. 13). This operation is called the entry cycle. The entry cycle has three variations: numeric, data descriptor, and clear.

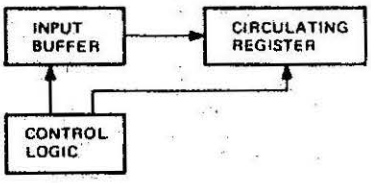


Fig. 13 Entry cycle block diagram

Before the entry cycle can begin, the eight bits of the data character must be received from the TCU, and the circulating register must be starting a new cycle. A cycle is 56 bit times long (approximately 389 μsec). The capacity of the circulating register is 14 four-bit characters.

The last bit of the data character from the TCU is signaled by TB8. The terms TCS, TCFF', and TB8 are anded to set the data entry period (DEP) flip-flop. Refer to figure 14 and figure 15. The DEP flip-flop permits the data in the input buffer to circulate until the circulating buffer is in position to accept the data. Setting the DEP flip-flop resets the SRD flip-flop and takes the place of SRD in holding the status at BUSY. The display logic remains in this state until the circulating register begins a new cycle.

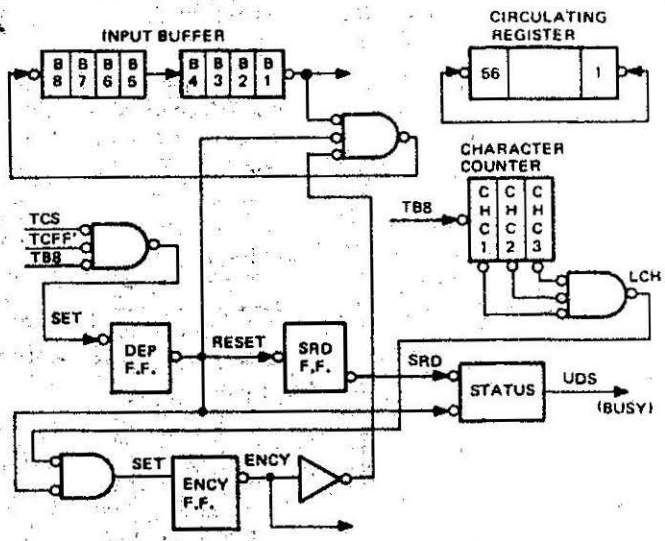


Fig. 14 Entry cycle initiation logic

The position of the 14 four-bit characters in the circulating register is indicated by the character counter. The character counter is a three-bit binary counter. The counter is advanced by one with each TB8 signal; therefore, each time the counter advances by one, the circulating register has moved two 4-bit character positions. When the counter has reached a count of seven, the circulating register has completed one full cycle and is ready to begin again.

The output of the counter is decoded to generate the term LCH (last character) when the count is seven. LCH and

M90 MODULE AND 790 UNIT NUMERIC/
DATA DESCRIPTOR DISPLAY

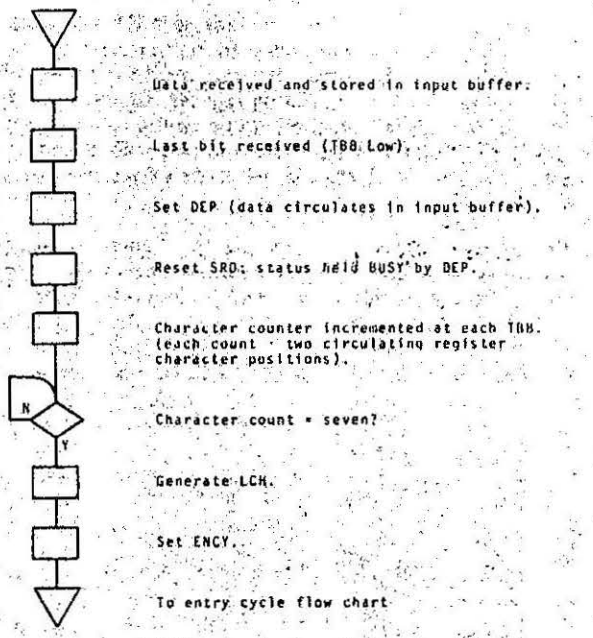


Fig. 15 Entry cycle initiation flow chart

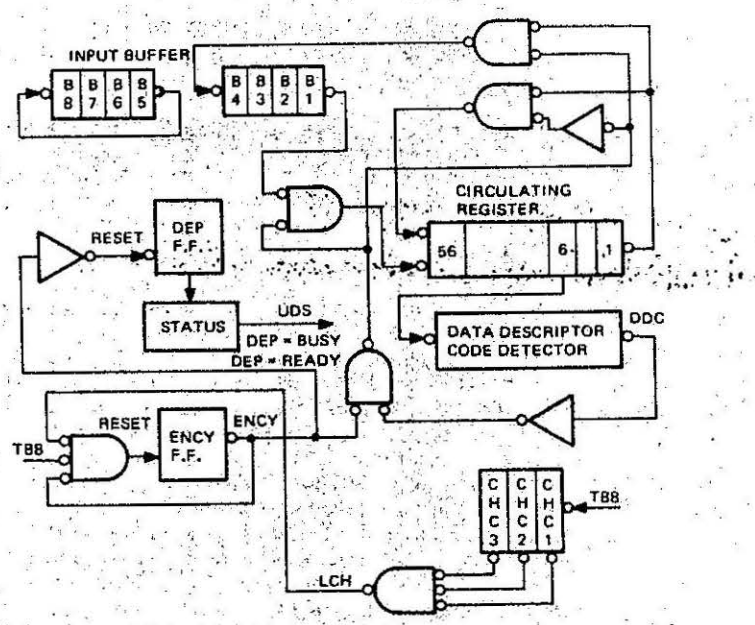


Fig. 16 Numeric data entry logic

DEP are anded to set the entry cycle (ENCY) flip-flop. The ENCY flip-flop inhibits the input buffer from cycling and begins the entry cycle.

The sequence of events during the entry cycle depends on whether the contents of the input buffer is numeric data, descriptor data, or whether the display is to be cleared.

NUMERIC ENTRY

Prior to setting the ENCY flip-flop, the content of bit position 1 of the circulating register is gated into position 56. Setting the ENCY flip-flop allows data to be transferred from the input buffer into the circulating register. When numeric data is to be entered into the circulating register, the content of B1 of the input buffer is shifted into position 56 of the circulating register as the content of position 1 is shifted into B4 of the input buffer. Figure 16 depicts the logic necessary to enter numeric data into the circulating register. The flow chart for this operation is shown in figure 17.

The shifting of the contents of the circulating register through the four least significant positions of the input buffer effectively lengthens the circulating register by four bits. Since the timing is based on the 56-bit length of the circulating register, the addition of four bits causes the numeric data to be shifted one position to the left. If, for example, the display has a 1 in the right most numeric position and a 2 is sent to the module, the 2 is displayed in the rightmost position and the 1 is displayed in the second position from the right.

The shifting through the input buffer continues until the entry cycle is complete (circulating register shifted 56 times) or until a data descriptor character is recognized.

In display modules combining a total of 14 numeric tubes and descriptor modules (for example the M-90-3-280), the numeric characters are prevented from shifting into a data descriptor character position, and data descriptor characters are prevented from being shifted to the left by generation of the term DDC. DDC (data descriptor code) is generated when a data descriptor character is recognized. DDC prevents the character from being shifted through the input buffer and reroutes the bit in position 1 of the circulating register into position 56. If shifting through the input buffer is allowed, the wrong descriptor message would light and more than one descriptor message in a given column may light, causing damage to the descriptor assembly.

In an all-numeric display module such as the M-90-1-748 or the numeric half of the M-90-3-270, the rerouting of the bit in position 1 of the circulating register directly into position 56 instead of through the input buffer is delayed until the entry cycle ends (ENCY flip-flop reset). The ENCY flip-flop is reset when the term LCH is generated 56 bit times after the entry cycle is initiated. When the ENCY

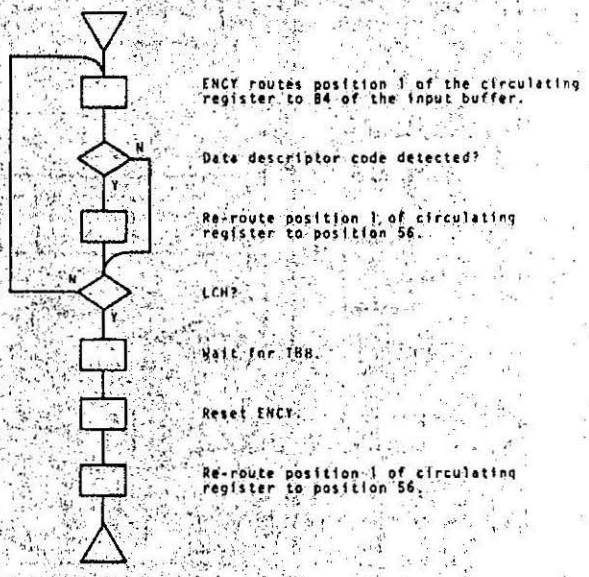


Fig. 17 Numeric data entry flow chart

flip-flop is reset, the data entry period (DEP) flip-flop resets to signal the end of the data entry period by switching the status from BUSY to READY.

The TCU is free to issue another function to the M-90 after the status returns to READY.

DATA DESCRIPTOR ENTRY

When an accept data descriptor character function is received from the TCU, the display module waits for the eight-bit data descriptor code to be sent. When the code is sent, the first four bits of the code are stored in the four most significant positions of the input buffer (B5 through B8). These four bits are used to determine which descriptor module (column) contains the message to be displayed. The most significant four bits of the data descriptor character are stored in bit positions B1 through B4 of the input buffer. These four bits determine which message (row), if any, within a column is to be lit. During the entry cycle, the row address is entered into the circulating register at a time determined by the column address. The row address remains in that position of the circulating register until a clear display function is issued or until another data descriptor code with the same column address is received.

When the ENCY flip-flop is set to start the entry cycle, the column address stored in B5 through B8 of the input buffer is circulated from B5 through a half-adder to B8 as shown in figure 18. Every four bit times (TB1 and TB5), the term TBC is generated to increment the column address by one. Each time the column address is incremented, a new column position in the circulating register is in position to be loaded. When the column address is incremented to a count of 14, the term DDA is generated to indicate that the circulating register is in position to accept the row address

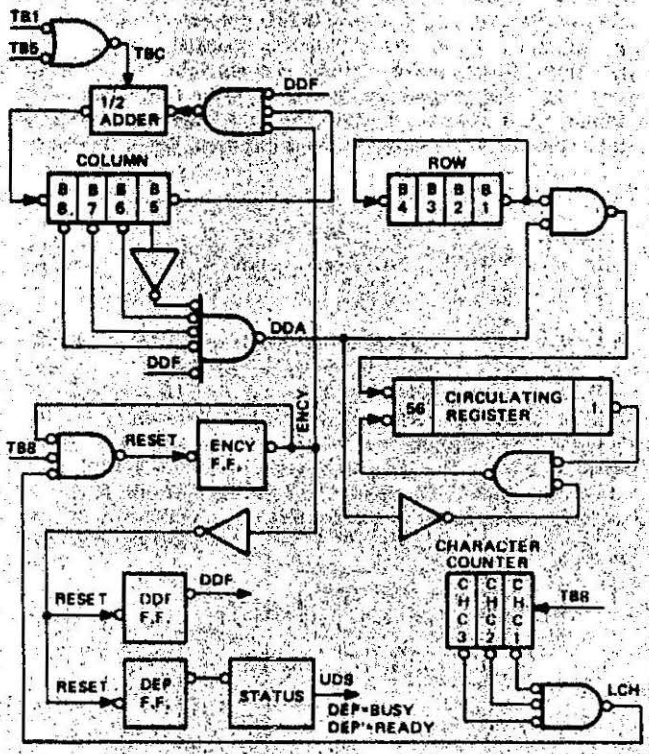


Fig. 18 Data descriptor entry logic

from the input buffer. The row address in B1 through B4 of the input buffer is entered into the circulating register through position 56. After the four bits of the row address are entered into the circulating register, the portion of the input buffer containing the column address is incremented, resetting DDA. The contents of the input buffer are prevented from entering the circulating register when DDA is reset.

The entry cycle outlined in the flow chart in figure 19 continues until the character counter reaches the count of seven. This generates LCH which, along with TB8, resets the ENCY flip-flop. When ENCY is reset, the DDF flip-flop and the DEP flip-flop are reset. The status to the TCU changes from BUSY to READY when DEP is reset.

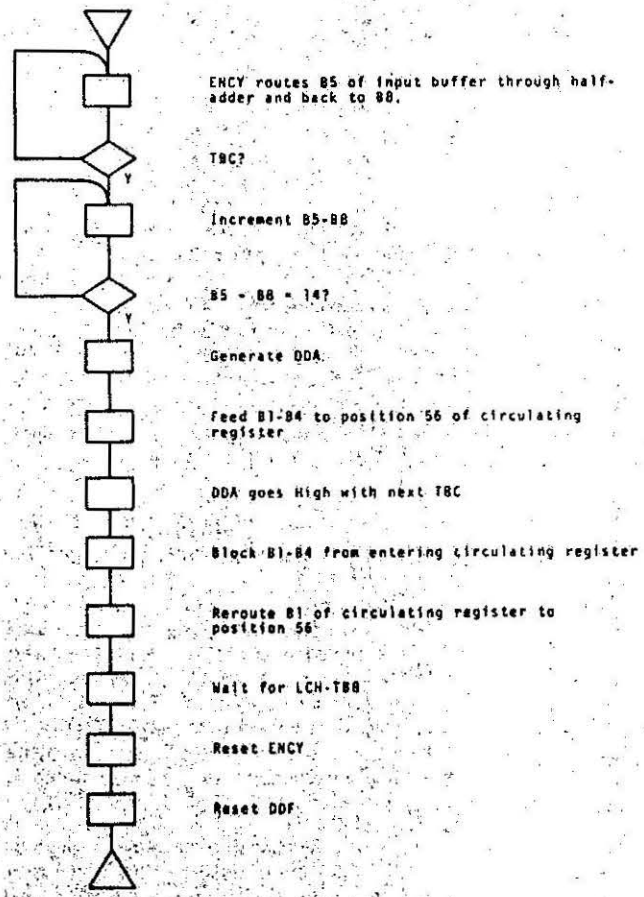


Fig. 19 Data descriptor entry flow chart

CLEAR ENTRY

The two clear functions, clear entire display function and clear numerics only function, clear the numerics and the decimal point but only the clear entire display function can clear the data descriptors. To clear any column in a display, a binary 15 (hex F) is entered into that column position in the circulating register. The binary 15 is decoded as a blank or null position by the display decode logic.

When either of the clear display functions is issued to a display module, the data entry period (DEP) flip-flop and the clear (CLR) flip-flop are set. Setting the DEP flip-flop causes the BUSY status to be sent to the TCU and allows the entry cycle (ENCY) flip-flop to set when the character counter reaches a count of seven (LCH generated).

...hen the ENCY flip-flop sets, the clear entry cycle begins. The bit from position 1 of the circulating register is routed back to position 56 as shown in figure 20. Logic ONE is forced into each bit position of the circulating register by holding position 56 Low. The data descriptor code detector is constantly monitoring the data in the circulating register for a data descriptor code. When the data descriptor code is detected, the term DDC is generated.

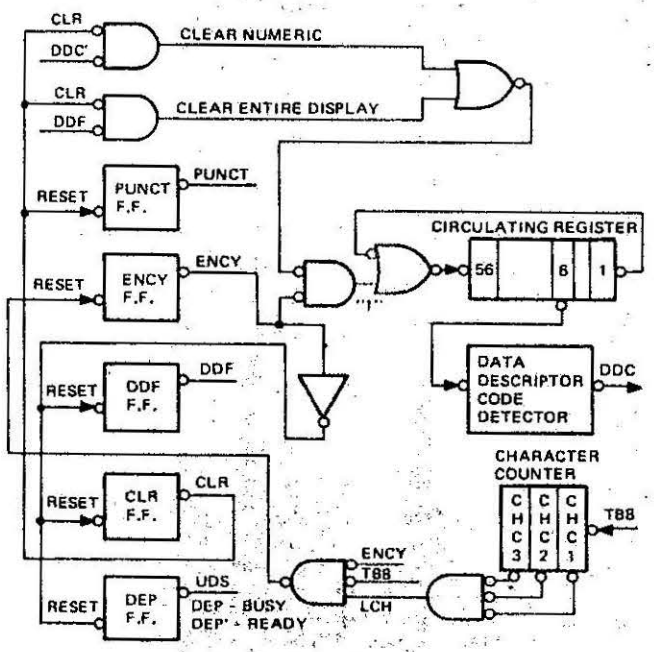


Fig. 20 Clear entry cycle logic

If a clear numeric only function is being performed, the forcing of logic ONE into each position is inhibited when DDC is generated. The content of position 1 is input to position 56. The content of the next character position (four bits) is decoded; and, if the character is a numeric, the bits of the character are forced to logic ONE as outlined in figure 21.

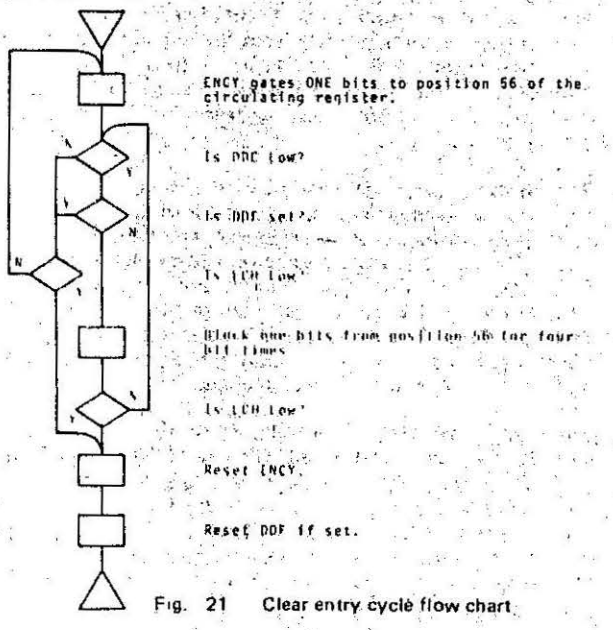


Fig. 21 Clear entry cycle flow chart

All bit positions of the circulating register are forced to logic ONE without regard to DDC if a clear entire display function is issued.

When the entry cycle ends (ENCY reset), the contents of the circulating register are recirculated from position 1 to position 56, the clear (CLR) flip-flop is reset, and the data entry period (DEP) flip-flop is reset. The status reverts to READY when the DEP flip-flop is reset.

DATA DISPLAY

The data display logic is made up of the elements shown in figure 22: the 56-bit circulating register, the segment decoder, the multiplexer, the output buffer, and the display strobe counter.

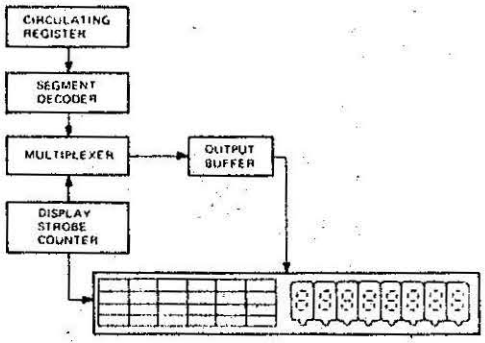


Fig. 22 Data display logic block diagram

Each of the 14 four-bit characters in the circulating register is loaded into the segment decoder. The segment decoder generates a new code from the four-bit code and outputs the code to the multiplexer. The strobe counter output, which determines the display sequence for numeric tube segments and data descriptor rows, is also output to the multiplexer. The multiplexer determines if a row or segment is to be displayed during the strobe time received from the strobe counter. The information from the multiplexer is loaded into the output buffer. The output buffer holds the information for one strobe time, then accepts the information for the next rows and segments to be displayed. This sequence is outlined in the flow in figure 23.

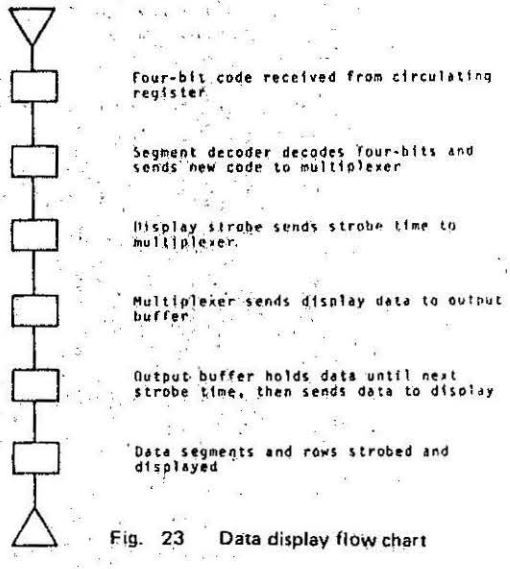


Fig. 23 Data display flow chart

CIRCULATING REGISTER

The circulating register is a 56 bit dynamic register. The contents of the register are divided into 14 four-bit characters. These characters can be either numeric codes or data descriptor codes. The characters are constantly being circulated from position 1 to position 56. During numeric data entry the effective length of the register is extended to include the four least significant bits of the input buffer.

To display all of the data contained in the circulating register, the register must circulate eight times (one cycle = 56 bit times or 389 μsec.). One segment of each numeric tube and/or one row of each data descriptor column may be lit for each cycle of the circulating register. Although each tube segment to be lit is lit for only 389 μsec. out of 3.12 msec. (eight cycle times) no flicker is apparent. Each data descriptor to be lit is lit for two out of the eight cycles.

SEGMENT DECODER

The segment decoder shown in relation to the other display logic in figure 24 takes each four-bit character from the circulating register and converts the code into a nine-bit code to be used by the multiplexer.

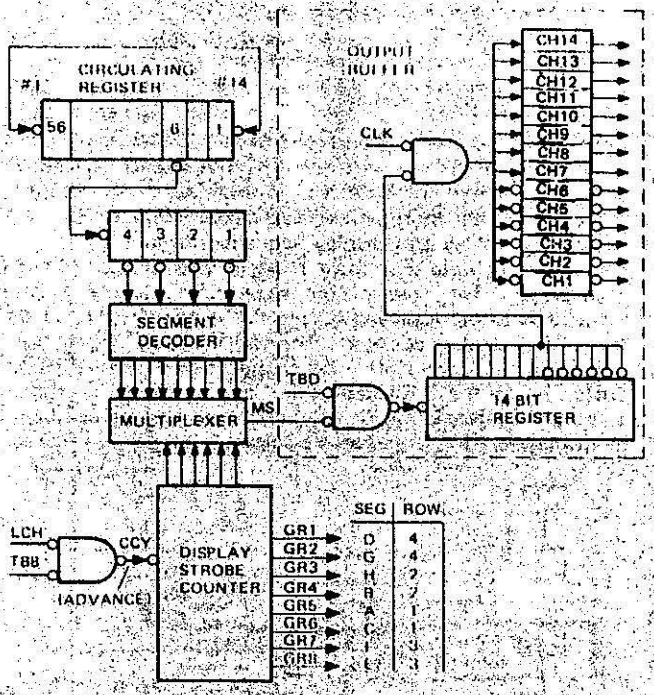


Fig. 24 Data display logic

During each register cycle (shown in fig. 25), data from position 6 of the circulating register is input serially to a four-bit register. After four bit times, a complete data character is in the register. The register feeds the four bits to the segment decoder in parallel. The decoder converts the four-bit code to a nine-bit code and forwards the nine-bit code to the multiplexer.

Each of the 14 characters in the circulating register is decoded by the segment decoder and input to the multiplexer. After the fourteenth character is processed

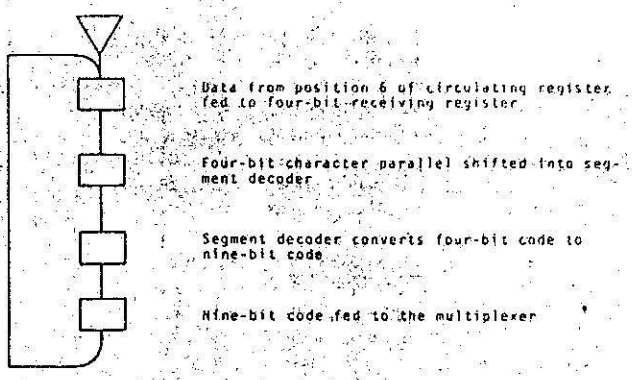


Fig. 25 Segment decoder flow chart

through the segment decoder, a new cycle begins. The cycles are repeated as long as power is applied to the display module.

In addition to the four bits input to the segment decoder from the circulating register, another input is provided. The input is DCT (decimal timing) as shown in figure 26. When DCT is Low the nine-bit output from the segment decoder is altered to include the decimal point. DCT is Low when the PUNCT flip-flop is set, the character counter is at 12, and TB5 is Low. When the character counter is at 12, the third numeric character position from the right is being decoded.

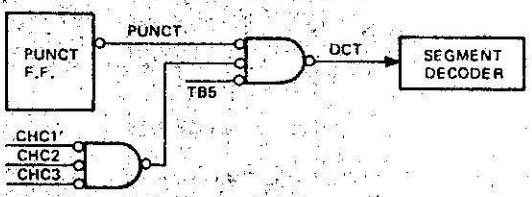


Fig. 26 Decimal encode logic

MULTIPLEXER AND DISPLAY STROBE COUNTER

The multiplexer requires two inputs before it can perform its function: a segment code from the segment decoder and a strobe count from the display strobe counter. The multiplexer combines these inputs to determine which data descriptor rows and/or tube segments are to be strobed during the next cycle.

The strobe counter determines which data descriptor row and/or tube segment may be strobed during any cycle. The counter is a three-bit binary counter. The counter shown in figure 27 is incremented each time the cycle clock term CCY goes Low. CCY goes Low at the beginning of each circulating register cycle. The counter counts from 000_2 through 111_2. When the counter is incremented back to 000_2, eight cycles of the circulating register are completed and all characters have been displayed.

There are two sets of outputs from the display strobe counter. One set (G1 through G3 and G1' through G3') is input the multiplexer. The other set (GR1 through GR8) is input to the display circuitry to strobe the data descriptor rows and/or tube segments. Each of the four data descriptor rows are strobed twice during eight cycles of the circulating register as compared to one strobe per tube segment during the same period.

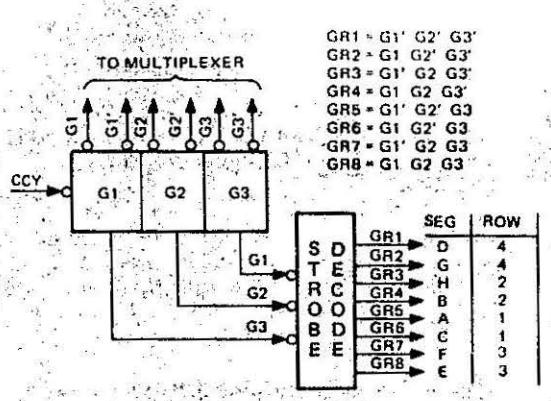


Fig. 27 Display strobe counter logic

The multiplexer uses the G1 through G3 and G1' through G3' outputs along with the nine-bit segment decoder output to determine which tube segment and/or data descriptor row is to be strobed during the next cycle. For example, when the numeric tube E segments and/or the data descriptor 3 rows are being strobed (GR8 time), each four-bit character from the circulating register is being decoded by the segment decoder. The multiplexer takes the nine-bit output from the segment decoder for each character and examines the nine-bit code to determine if a numeric tube D segment or a data descriptor 4 row is to be lit during the next cycle (GR1 time). If a numeric tube D segment or a data descriptor 4 row is to be lit during the next cycle, the output of the multiplexer, MS, switches Low to the output buffer. MS switches Low for each display position which requires the lighting of a numeric tube D segment or data descriptor 4 row during the next cycle. The sequence of operation of the strobe counter and multiplexer is shown in figure 28.

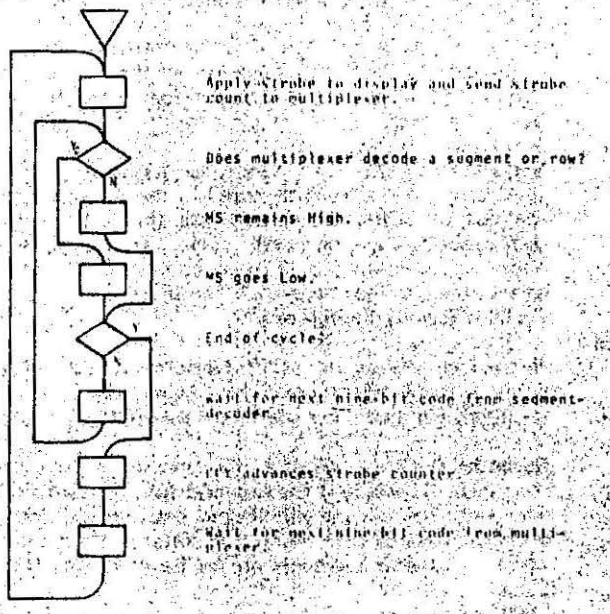


Fig. 28 Strobe counter and multiplexer operation flow chart

OUTPUT BUFFER

Data characters from the 56-bit circulating register are decoded and multiplexed with a timing signal (strobe count) to provide a one-bit input to the output buffer. A bit is input to the first of the two registers in the output buffer for each of the 14 display positions. When all 14 bits are entered into the dynamic register (one cycle of the circulating register completed), the 14 bits are shifted in parallel into a 14-bit static register (CH1 through CH14). The static register outputs provide input to the tube grid drivers and the data descriptor lamp drivers.

While the tube segments and/or data descriptor rows determined by the static register outputs (CH1 through CH14) and the strobe counter outputs (GR1 through GR8) are being lit, the contents of the circulating register are being examined to determine which character positions require lighting of tube segments and/or data descriptor rows during the next cycle. The sequence of data entry and movement within the output buffer is outlined in the bubble flow in figure 29.

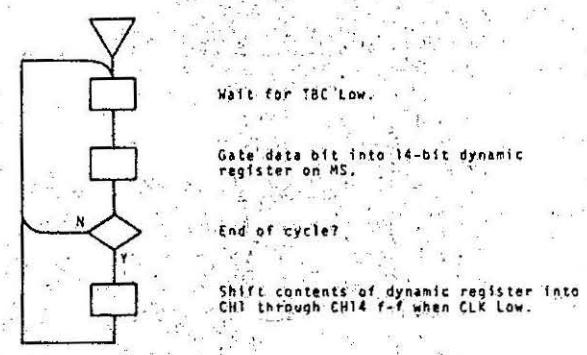


Fig. 29 Output buffer operation flow chart

LOGIC SUMMARY

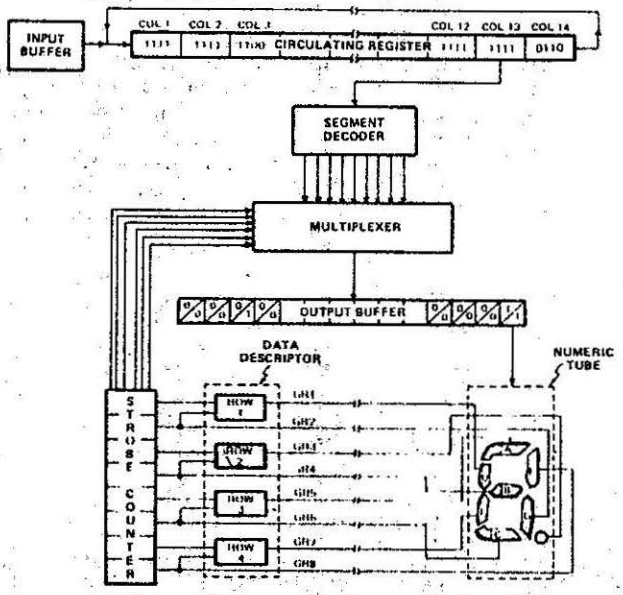
The logic incorporated in the M-90 display modules can perform six TCU-issued functions: punctuate, accept data descriptor character, accept numeric character, punctuate and accept numeric character, clear entire display, and clear numeric portion only.

Following receipt of any of the three accept character functions, the logic prepares to receive an eight-bit data character from the TCU. When the data character is received, it is shifted into a 56-bit circulating register. Each of the 14 four-bit characters is decoded then compared to the tube segment and data descriptor row count by the multiplexer. If the multiplexer determines that a tube segment or data descriptor row is to be lit for the character position decoded, the multiplexer inputs a ONE bit to the output buffer. A ZERO bit is input if a tube segment or data descriptor row is not to be lit.

The circulating register contents are decoded eight times, once for each numeric tube segment or twice for each data descriptor row. During each cycle, all 14 characters are examined and a ONE bit is stored in the dynamic register of the output buffer for each position requiring the same tube segment to light or data descriptor to light. After all 14 characters are examined, the contents of the dynamic register are shifted into a 14-bit static register. The output of the static register flip-flops provide input to tube grid drivers and data descriptor row drivers.

An example of segment decode and display is shown in

figure 30. The display module is an M-90-3-280. In the example all descriptor positions are blank except for the third column and the fourteenth column. The third column contains a data descriptor code for row two, and the fourteenth column contains the code for the numeric six. The state of the output buffer during the fourth cycle is shown.



	ROW DECODED/DISPLAYED	SEGMENT DECODED/DISPLAYED
1st cycle		G/D
2nd cycle	2/	/G
3rd cycle	2/2	B/
4th cycle	/2	A/B
5th cycle		C/A
6th cycle		F/C
7th cycle		/F
8th cycle		D/

Fig. 30 Display operation

A brief description of the display operation during each cycle of the circulating register follows.

First Cycle — During the first cycle, the 14 characters of the circulating register are examined to determine if any data descriptor module (column) 4 row or if any numeric tube G segments are to be lit during the next cycle. A ONE bit is stored in the dynamic register of the output buffer for each row or segment to be lit. The rows or segments decoded during the eighth cycle are displayed during this cycle. In the example, while the tube D segment is lit, the characters are examined for G segments to be lit during the second cycle. No data descriptor rows are decoded or displayed.

Second Cycle — During the second cycle, the data descriptor 4 rows and the numeric tube G segments decode during the previous cycle are displayed while the characters are decoded for the data descriptor 2 rows and numeric tube H segments (decimal points) to be displayed during the third cycle.

The data descriptor 2 row in column 3 is decoded and the G segment of the numeric tube in column 14 is lit in the example display. The D segment lit during the first cycle is extinguished.

Third Cycle — The circulating register contents are decoded for numeric tube B segments and data descriptor 2 rows during the third cycle. The numeric tube H segments and data descriptor 2 rows previously decoded are displayed during this cycle.

In the sample operation a B segment for column 14 and a 2 row for column 3 are decoded while the 2 row in column 3 is lit. The G segment lit during the second cycle is extinguished.

Fourth Cycle — Any numeric tube B segments or data descriptor 2 rows decoded during the third cycle are displayed during the fourth cycle. The numeric tube A segments and data descriptor 1 rows for display during the fifth cycle are decoded in the fourth cycle.

Row 2 of the data descriptor in column 3 and the B segment of the numeric tube in column 14 are lit in the example while a ONE bit is stored in column 14 of the dynamic register of the output buffer to light the numeric tube A segment during the fifth cycle.

Fifth Cycle — During the fifth cycle, the multiplexer stores a ONE bit in the output buffer dynamic register for each data descriptor column in which row 1 is to be lit and for each numeric tube in which segment C is to be lit. All data descriptor 1 rows and numeric tube A segments decoded during the fourth cycle are displayed during this cycle.

In the example, no data descriptor rows are decoded or displayed. While the A segment of the numeric tube in column 14 is lit, the C segment for the same column is being decoded.

Sixth Cycle — The data descriptor 1 row and the numeric tube C segment ONE bits stored in the dynamic register of the output buffer are shifted into the static register and displayed during the sixth cycle. The data descriptor columns containing a 3 row code and numeric tubes containing an F segment code are decoded during the sixth cycle of the circulating register.

In the example, segment C of the numeric tube in column 1 is lit and the F segment for display in cycle seven is decoded. No data descriptor rows are displayed or decoded.

Seventh Cycle — During the seventh cycle, the data descriptor 3 rows and the numeric tube F segments are lit. The contents of the circulating register are decoded to determine which data descriptor column 3 rows and which numeric tube E segments are to be lit during the eighth cycle.

The F segment of the numeric tube in column 1 in the example is displayed during the seventh cycle. During the character decode, no numeric tube E segments are decoded, nor are any data descriptor 3 rows decoded.

Eighth Cycle — The numeric tube E segments and data

M90 MODULE AND 790 UNIT NUMERIC/DATA DESCRIPTOR DISPLAY

descriptor 3 rows decoded and stored in the dynamic register of output buffer are shifted in parallel to the static register. After the data is shifted into the static register, the corresponding segments and rows are displayed. The characters in the circulating register are decided to determine if a 4 row is to be displayed in any data descriptor column or if a D segment is to be displayed in any numeric tube.

In the example, there are no data descriptor rows or numeric tube segments to light during the eighth cycle. The D segment of the numeric tube in column 1 is decoded for display during the next cycle but there are no data descriptor rows to be lit during the next cycle.

The eight cycles are repeated continuously as long as the parent unit clock and power supply is operational. The decode and display of the circulating register contents continue even while data is being entered from the input buffer.

ELECTRICAL DESCRIPTION

In the logic description, the operation of the MOS/LSI arrays is explained. In order to actually light numeric tube segments and data descriptor rows, drive circuits are required. The drive circuits are made up of discreet components or hybrid circuit packages. The 790 remote display contains the same type of display drive circuits as the display modules, but the remote display requires line drivers for the common port signals.

DISPLAY DRIVE CIRCUITS

NUMERICS

The numeric display tube is a vacuum tube with a directly heated cathode, a control grid, and eight phosphorcoated anode segments. The control grid mesh and filament wire are located in front of the anode segments, but are not visible at a normal viewing distance.

The tube is suited to the scanning mode of operation of the display because it functions as an and gate. An anode segment lights only when both the segment and the control grid are simultaneously positive with respect to the cathode. Each of the anode segments is controlled by a driver whose input is one of the eight strobe counter outputs (GR1 through GR8). The grid is controlled by a driver whose input is one of the output buffer outputs (CH1 through CH14).

The circuit in figure 31 shows a typical numeric tube with anode drivers and grid driver. There is one anode driver for the corresponding anode in all numeric tubes. For example, the A segment anode in each numeric tube is driven at the

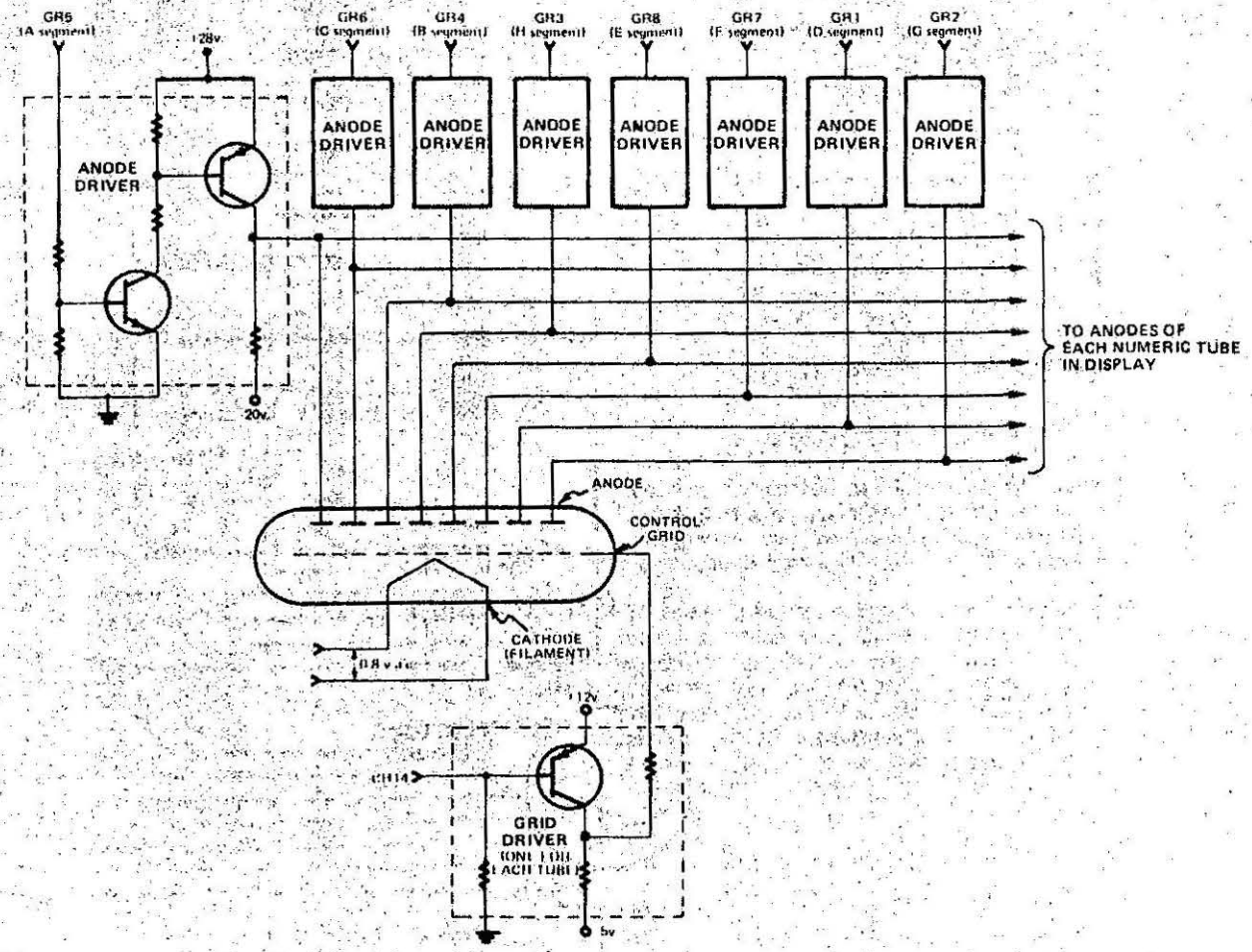


Fig. 31 Numeric tube drivers

same time by the same driver. A separate grid driver is provided for each numeric tube in the display.

As shown in figure 31, the cathode (filament) has 0.8 v.a.c. dropped across it. This 0.8 v.a.c. is referenced to -20 v.d.c. The grid driver input is normally High (+12 v.d.c.) which applies approximately -5 v.d.c. (referenced to -20 v.d.c.) to the grid to prevent the tube from conducting. The anode driver output is -20 v.d.c. when the driver input is Low (-6.8 v.d.c.).

When the A segment of the numeric tube in column 14 is to be lit, GR5 goes High and CH14 goes Low. The output of the anode driver switches from -20 v.d.c. to +28 v.d.c. The grid driver output switches from -5 v.d.c. to +12 v.d.c. With both the grid and the anode positive with respect to the cathode, the tube conducts and the A segment lights. The segment remains lit for 56 bit times (389 μsec.).

DATA DESCRIPTORS

The data descriptors are illuminated by incandescent lamps. Each module contains four lamps. Each lamp illuminates one message. The lamps are numbered 1 through 4 with lamp 1 at the top of the module and lamp 4 at the bottom.

The lamp driver circuits shown in figure 32 are representative of those used in all M-90 data descriptor displays. When either of the strobe counter inputs (GR5 or GR6) to the row 1 driver is High (+12 v.d.c.), the output of the driver is at +28 v.d.c. This +28 v.d.c. is applied to the row 1 lamps in all data descriptor columns.

Before any of the row 1 lamps can light, the darlington transistor used as the data descriptor column driver must be biased on. To bias the darlington transistor on, the input signal from the output buffer must go High. When the darlington transistor is conducting, current flows through the isolation diode, lamp, and transistor to ground to light the lamp. Since the data descriptor rows are decoded twice during every eight circulating register cycles, any lamp lit is lit for 778 μsec.

The isolation diode in series with each lamp prevents back circuits.

A preheat input is provided to every data descriptor column in some M-90 modules. The preheat input is High for 7 μsec. out of every 16 cycles. This time is short enough to allow the lamp filaments to heat but not to be visible. Preheating the lamp filaments lengthens the life of the lamps.

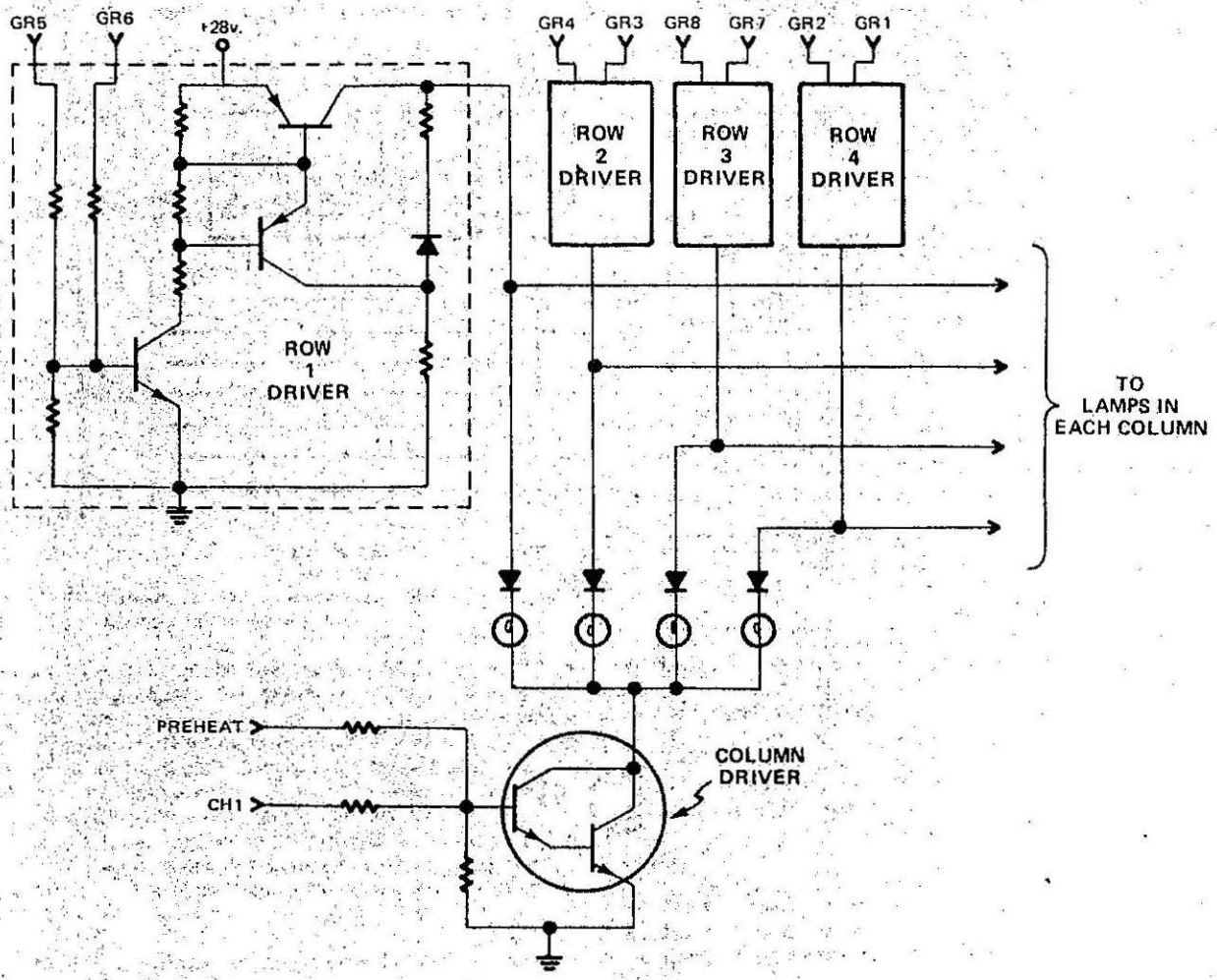


Fig. 32 Data descriptor drivers

790 REMOTE DISPLAY

The 790 remote display, like all M-90 modules, is operated as a peripheral on the terminal control unit (TCU) common port. Although this unit has only 10 columns (six numeric tubes and four 4-message data descriptor modules), the 790 operation is the same as any 14 column display module. The numeric tubes are provided with input from the six least significant character positions of the circulating register, and the data descriptor inputs are provided from the four most significant character positions of the circulating register. It is the responsibility of the TCU firmware to ensure that data is not entered into the unused character positions of the circulating register.

The 790 has two circuit boards. One contains the numeric tubes, the data descriptor modules, and the driver circuits. The remaining board contains the four MOS/LSI arrays, some discrete components, and line driver circuits.

LINE DRIVER CIRCUITS

All control signals from the TCU to the 790 except phase 1, phase 3, and TCIR are inverted by the common port connector board line drivers. The line receiver circuits on the 790 logic board converts the inverted signals back to MOS/LSI compatible levels.

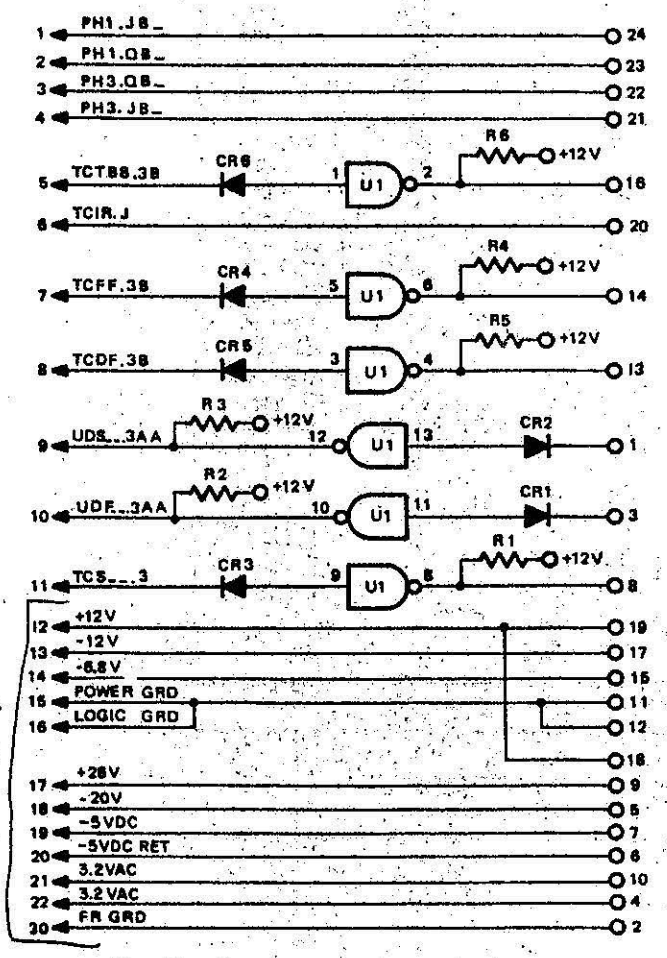


Fig. 33 Common port connector board circuit

The UDS and UDF signals are inverted in the 790 before being sent to the TCU. These signals are inverted back to MOS/LSI compatible signals by circuitry on the parent unit line driver (figure 33). The signals are then applied to the common port.

The timing for control lines and clock signals as they appear at the 790 end of the 10 foot connector cable are shown in figure 34.

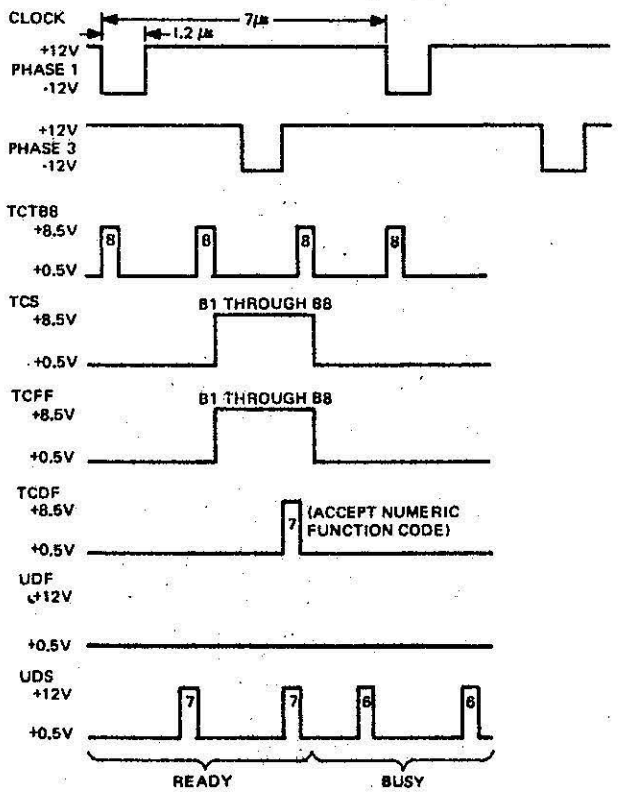


Fig. 34 Control line and clock timing

SERVICE INFORMATION

Since each model of the M-90 display module is different, complete diagnostic information is not provided here. This information can be found in the Technical Information Handbook or Manual for the unit using the M-90.

The various models are provided with a test input at pin 29 of the common port connector. When -6.8 v.d.c. is applied to pin 29, all data descriptor rows are lit and all numeric tubes extinguished. All numeric tube segments are lit when +12 v.d.c. is applied to pin 29. To prevent damaging the plastic data descriptor modules, -6.8 v.d.c. should not be held on pin 29 more than 5 seconds out of every 30 seconds.

Display Jumper Test.

Display Voltages

Bottom left on display plug to
+12V on TB2-1
-6.8 on TB2-5.

*Touch near back left of Display BCB.